IN THE SPECIFICATION

The paragraph beginning on page 11, line 21 is amended as follows:

Figure 5A again shows the p-channel flash memory cell 501, or p-channel static device 501, having a floating gate oxide of less than 50 Angstroms according to the teachings of the present invention. As shown in Figure 5A the floating gate 504 has a bottom surface area 509 in contact with the oxide layer, or floating gate oxide 505. In one embodiment according to the teachings of the present invention, the bottom surface area has an area of approximately 10^{-10} cm^2. Figure 5A illustrates the source side tunneling for F-N tunneling erase or thermally assisted tunneling charge leakage of stored electrons off of a polysilicon floating gate 504. In one embodiment, the polysilicon floating gate 504 is an n-type polysilicon floating gate 504, such as an n+ polysilicon floating gate 504. In an alternative embodiment, the polysilicon floating gate 504 is an p-type polysilicon floating gate 504, such as an p+ polysilicon floating gate 504. In another embodiment, the polysilicon floating gate 504 is a polysilicon-germanium floating gate 504. According to the teachings of the present invention, an n-type polysilicon floating gate 504, such as an n+ polysilicon floating gate 504 is preferred rather than a p-type polysilicon or p-type polysilicon-germanium floating gate since the tunneling barrier for electrons is lower. Figure 5B is an energy band diagram which illustrates generally the thermally assisted tunneling or tunneling erase of charge from the floating gate 504 to the source 510, when the floating gate is driven to a negative potential by pulsing the control gate 502 to a negative voltage, where $\Delta V=Q/C$.